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Path Tracer for Transistor-level STA Setup using Synopsys NanoTime

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Abstract

In DRAM design, sign-off has been done using SPICE simulation, but as chip size increases and required specification becomes complicated, coverage issue arises. STA (Static timing analysis), which is commonly used to sign-off SoC (System on Chip), can resolve the coverage issue as it essentially does static analysis, but it is not easy to adopt STA on DRAM design due to characteristics of DRAM. In this work, we clarify why it is challenging to adopt STA on DRAM design: long runtime and difficulty in defining SDC (Synopsys Design Constraint), and propose a transistor level STA methodology to resolve this issue. Specifically, we propose a path tracer that traces nets between signal startpoints and endpoints while passing through latches, and generates proper SDC on the traced nets, by which the long runtime can be reduced by reconstructing a small netlist only using the traced nets and performing STA on the small netlist, and the difficulty in writing SDC can be resolved by automatic SDC generation on traced nets. Through experiments with sets of critical paths, it is shown that our proposed path tracer is able to trace nets and generate SDC in a reasonable time, which makes STA on DRAM design to be possible.

1. Motivation: Challenges in adopting STA to DRAM Timing Sign-off

- Why we are trying to adopt STA on DRAM timing sign-off?
  - DRAM has been designed in *transistor-level* to highly optimize chip area.
  - *Dynamic simulation* (e.g. SPICE) is used for timing sign-off of DRAM.
    - Required Specification ⇑ → Chip size ⇑ , Timing margin ⇓ .
    - *Coverage issue* arises due to vector dependency.
  - Then, *how about **adopting STA to DRAM timing sign-off*** ?

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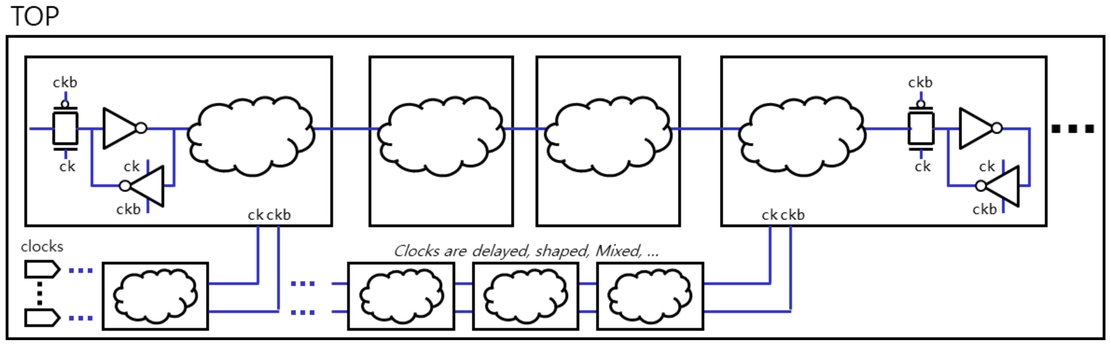
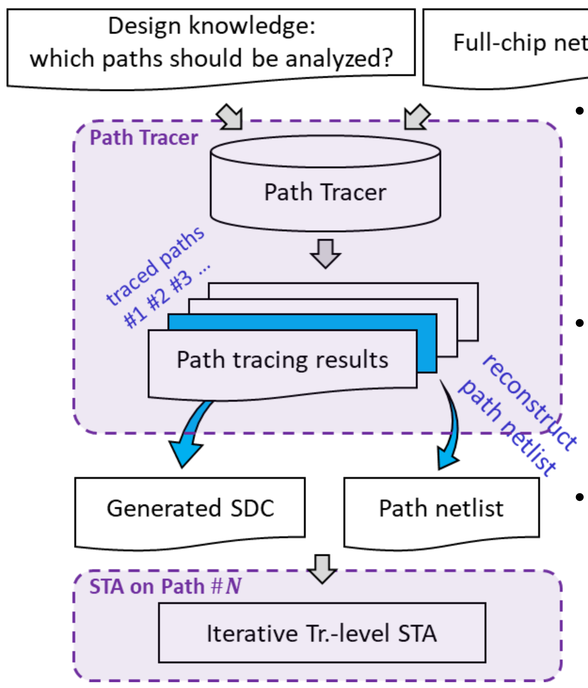
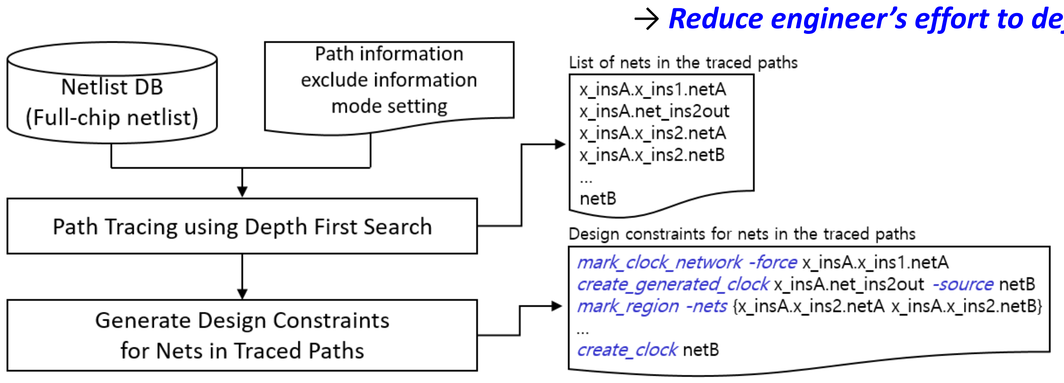


- Challenges introduced by characteristics of…
  - DRAM design:
    - No block spec., clock signals are shaped in multiple blocks → Full-chip STA
    - Large design size (# transistors > 15m) → *Long runtime (1d~)*
    - Complex clock scheme → *Difficulty in defining SDC*
  - Transistor-level STA:
    - No characterized standard cell, all transistors should be analyzed → *Long runtime*
    - No commercial EDA tools for SDC validation → *Difficulty in defining SDC*

2. STA Flow using Path Tracer



- Designer defines paths to be analyzed using STA
  - *Where the paths start from?*
  - *Where the paths end at?*
  - *Which latches the paths pass through?*
  - *Which nets should not be included?*
- Then, *Path Tracer*
  - Identifies paths between user specified points
  - Distinguishes clock and data
  - Analyzes connection of nets
- Finally,
  - Keep list of nets included in the paths
    → Used to reconstruct *smaller path netlist*, which inherently not include false path
    → ***Reduce STA runtime***
  - Generates sets of SDC required for STA
    → ***Reduce engineer's effort to define SDC***



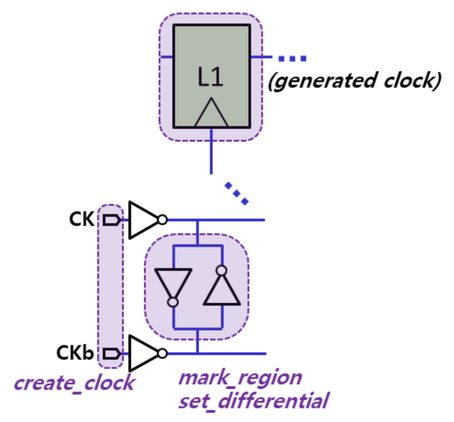
3. Results of Proposed *Path Tracer*

User given path information | *Results of Path Tracer*

	# of Startpoints	# of Through Latches	# of Endpoints	# of Traced Paths	# of Traced Nets	# of SDC Generated	Runtime [s]
Path #1	23	1453	454	27213	10687 (0.06%)	107	238
Path #2	8664	7667	32	403016	135554 (0.71%)	354	2950
Path #3	648	3880	33	48796	29062 (0.15%)	271	853
Path #4	648	8756	8704	443564	166444 (0.87%)	273	3930
Path #5	472	1833	65536	498812	126773 (0.66%)	153	76176
Path #6	480	732	12640	176527	55452 (0.29%)	85	2741
Path #7	480	761	3665	57392	46709 (0.24%)	142	407
Path #8	480	732	35	12524	16846 (0.09%)	85	335

(% of traced nets / total nets)

**** Generated SDC example:***



Summary

- **We propose a *methodology to boost up transistor-level STA on DRAM design*, which can…**
  - **Identify all existing paths between user specified points and keep list of nets included in the paths to reconstruct smaller netlist for the paths.**
  - **Analyze connection of nets in the paths while distinguishing whether each net is data or clock, and generate sets of SDC required for STA on the paths.**
- **Proposed methodology can contribute to reduce TAT (Turnaround Time) of timing-signoff on DRAM using STA by resolving issues of…**
  - ***Long runtime*, by *constructing smaller netlist that only contains paths to be analyzed* (+@, for accuracy & SI analysis).**
  - ***Difficulty in defining SDC*, by *providing sets of automatically generated SDC*, from which engineer can select among them.**